## **Amendments to the Specification:**

Please replace paragraph 2 on page 5 of the Specification with the following:

There are several variations of out-of-order or dynamic execution processors. An out-of-order execution processor is shown in Fig. 1. The out-of-order execution processor includes a dynamic portion 105 of the processor 100 including a register-renaming unit 110, which maps between temporary and architectural files, a reorder buffer 120, a number of reservation stations 130, and a number of execution units 140. A bus 115 couples the register renaming unit 110, the reorder buffer 120, the reservation stations 130, the execution units 140, and a scoreboard 132152 together and to the remaining portions of the processor that are not shown.

Please replace paragraph 1 on page 15 of the Specification with the following:

Fig. 5C shows one embodiment of processing the instruction in the reorder buffer in a limited predicate slip, out-of-order CPU. For each entry in reorder buffer, processed in order, the result of the instruction is checked for availability in process block 528. If the result is not ready, then the update of the reorder buffer is stalled until the result is ready. If the result is ready, the source predicate is checked for availability in process block 530. If the source predicate is not ready, then the update of the reorder buffer is stalled until the source predicate is ready. If the source predicate is ready. If the source predicate is ready. If the source predicate is ready, then the predicate whether the predicate is true or not is determined in process block, 53532. If the predicate is true, then the result of the instruction is written to the register file in block 534. The scoreboard is then cleared in process block 536 and the reorder buffer entry for the instruction is cleared in

process block 538. If the predicate is false (not true) in process block 532, the result of the instruction is discarded in process block 540 and the scoreboard is then cleared in process block 536 and the reorder buffer entry for the instruction is cleared in process block 538.